國立台灣大學技術行銷表

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產品/技術名稱	以鹼式法及水熱程序製備含顆粒直徑小於 10 奈米之膠體液及介電值小於 2 之中孔型二氧化矽薄膜
發明人/單位	萬本儒，呂信諺，台灣大學化工系
產品/技術說明	隨著積體電路尺寸的縮小，電阻-電容時間延遲(RC time delay)的問題益顯嚴重，有必要使用介電係數更低的絕緣材料。而現今工業所使用的二氧化矽(SiO_2)材料之介電係數最小約為 2.3，已無法滿足解決此問題之需求。所以本專利申請所涵蓋之創新技術，是有關介電常數小於 2 而且機械強度足夠強的孔洞型低介電薄膜材料的製造程序，未來將能幫助積體電路工業解決相關問題。
應用範圍	半導體及積體電路工業
產品/技術優勢	1. 本發明製備出介電常數小於 2 且機械強度高(彈性係數大於 10GPa，硬度大於 1GPa)的孔洞型二氧化矽薄膜。 2. 本發明是合成非結晶性的二氧化矽小顆粒(小於 10 奈米)，因此利用其所製備出的薄膜，整體機械性質較佳。 3. 本發明製備程序簡便，相較於過去之文獻及專利的製程方法所需時間至少 7 天以上，本發明僅需 2.5 天，因此可有效的解決製程冗長之問題且可大幅降低製備成本。
市場潛力	ITRS2008(http://www.itrs.net/)年所公佈的半導體需求顯示，當半導體製程邁向 32 奈米時，低介電係數材料的介電係數必須在 2.4 以下，而到 20 奈米時(2015 年)，介電常數更需低至 1.9。而傳統所使用之介電材料離此目標仍有大段距離，因此可以肯定此材料於未來具有高度的應用潛力。
產品/技術 智財權保護方式	(由技轉室填寫)

(註：紅字為填表說明，請填寫時將其刪除)

Marketing Abstract of NTU's Invention Disclosure

Title	Preparing meso-porous silica film with dielectric constant less than 2 by using basic solution with particle sizes less than 10 nm from hydrothermal processes
Inventor (s)	Ben-Zu Wan and Hsin-Yan Lu, Department of Chemical Engineering, National Taiwan University
Brief Description	As the packing density of metal lines in semiconductors continues to increase, so does the problem of RC time delay become worse. The dielectric constant (*k* value) of the traditionally used inter-metal dielectric, dense silica (SiO_2), is around 4, which will soon be too large. As a result, a porous SiO_2 dielectric film with *k* value smaller than 2 is urgently required. However, the mechanical strength of the porous film is always not good enough to meet the requirements of IC industry. In order to meet the needs of practical application, the mechanical strength of the porous film should be improved immediately.
Fields of Application	The industry of integrated circuit (IC) manufacturing
Advantages	1. A porous SiO_2 dielectric film with *k* value < 2 and good mechanical strength, i.e., elastic modulus > 10GPa and hardness > 1GPa, has been produced. 2. The film was synthesized from a solution containing SiO_2 particles with size < 10 nm. Due to the small particles, the mechanical strength of the film was good. 3. The time period for manufacturing process of the film was only 60 h. In comparison with that of 168 h, at least, this process is much more efficient to cut down the cost of production.
Market Potential	ITRS 2008 established that the required value of the dielectric constant (*k* value) will be 1.9 as the gate length of CMOS devices approaches 20nm in 2015. However, the *k* value of the traditionally used intermetal dielectric, dense silica, is around 3.9, which is still far away to meet the required value. Therefore, it is definitely sure that the low-k film synthesized in this study is highly competitive.
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