國立臺灣大學技術行銷表

台大案號:_____(由產學合作中心填寫)

產學合作中心聯絡人：　　電話：　　e-mail：

產品/技術名稱	對稱時鐘樹之結構與合成
發明人/單位	施信瑋 與 張耀文
產品/技術說明	在高速晶片的同步系統中，擁有較小時鐘歪斜(clock skew)的時鐘樹(clock tree)可以有效改進時脈速度；隨著製程不斷進步，製程變異(process variation)對時鐘樹的影響也越顯著，使得時鐘歪斜的最佳化越來越困難。過去文獻上，大多數時鐘樹合成相關技術須仰賴時程模型(timing model)估算時鐘歪斜，而時程模型的精準度與複雜度就會主宰著時鐘樹合成技術的品質與效率。一般而言，較高精準度之模型能得到較小的時鐘歪斜，卻會使得合成時間非常長。常用的時程模型已越來越難滿足高速晶片對於精準度的需求，直接使用模擬(simulation)技術來估算時鐘歪斜變得似乎無法避免；這也就造成了時鐘樹合成所需的執行時間可能長達數小時，嚴重影響晶片設計流程(design flow)的收斂時間。 為克服精準度與效率之間的權衡問題，我們提出從結構上做最佳化的方式，即建立對稱結構(*symmetrical structure*)之時鐘樹，以完成時鐘歪斜最佳化。所謂的對稱結構，就是讓時鐘樹裡同一級的各處，其分枝數(number of branches)、繞線長度與加入的緩衝器(buffer)幾乎相同。如此一來，每一條從源點(clock source)到同步元件(clock sink)的路徑都有相似的配置。因此，不用透過模擬，也不需參考時程模型，時鐘歪斜就能很自然地被降低。此外，對稱性也能提升對製程變異之容忍度，使變異對時鐘歪斜的影響降低，以提升製造之良率。
應用範圍	積體電路電腦輔助設計、積體電路設計、晶圓製造
產品/技術優勢	1. 高準度：結構最佳化的方式不會有使用時程模型的誤差，而對稱結構能得到很小的時鐘歪斜 2. 快速：對稱結構的建立不需要使用模擬技術，因此執行效率遠快於其他使用模擬技術的合成方法 3. 具製程變異之韌性：由於時鐘樹裡每一條從源點到同步元件的路徑都有相似的配置，製程變異對時鐘歪斜之影響可以被降低

市場潛力	同步設計(synchronization system design)是當代晶片設計之主流，而此設計之同步系統需要好的時鐘樹來驅動。不同於過去的技術，對稱結構之時鐘樹可以有效降低時鐘歪斜與提升對製程變異之韌性；其結構之建立也能在不參考模擬資訊與時程模型的前提下迅速完成。此結構可以廣泛應用在積體電路設計領域上，包括積體電路電腦輔助設計、晶片設計、晶圓製造等都能使用此結構提升晶片之效能與生產良率。
產品/技術 智財權保護方式	

Marketing Abstract of NTU's Invention Disclosure

NTU's docket no:_____(由產學合作中心填寫)

CIAC contact：　　Tel：　　e-mail：

Title	Structure and Synthesis of Symmetrical Clock Trees
Inventor (s)	Xin-Wei Shih and Yao-Wen Chang
Brief Description	In high-performance synchronous chip design, a clock tree with small clock skew is essential for improving clocking speed. Moreover, as the process fast evolving, the clock skew optimization becomes harder under process variation. According to the existing literature, embedding simulation process into a clock-tree synthesis (CTS) becomes inevitable due to the insufficient accuracy of timing models. Consequently, the runtime for CTS becomes prohibitively huge as the complexity of chip designs grows rapidly. Therefore, we propose a new structure, called *symmetrical structure*, to overcome the difficulty. In this structure, the number of branches, the wirelength, and the inserted buffers are almost the same at each level of the symmetrical clock tree. It is nature that the clock skew could be minimized when the configurations of all paths from the clock source to sinks are similar without referring to simulation information or using timing model. In addition, since the clock tree is symmetrical, the process-variation effect can also be reduced naturally.

Fields of Application	computer aided design for VLSI (electronic design automation), chip design, wafer foundry
Advantages	1. Good accuracy: Very small clock skew can be achieved by the symmetrical structure, which is constructed without including timing models and thus has no timing-model error. 2. Good efficiency: The construction of symmetrical structure is performed without including simulation. Therefore, the runtime is much shorter than clock-tree synthesis techniques with including simulation. 3. High tolerance for process variation: Since the configurations of all paths from the clock source to sinks are similar, the process-variation effect can also be reduced naturally.
Market Potential	The synchronization system design is the main technique in modern VLSI chip design. In the design, the system has to be driven by a good clock tree for synchronization. Unlike previous techniques, the symmetrical structure can effectively minimize clock skew against process variation. Moreover, this structure can also be fast established without referring to simulation information or using timing model. The symmetrical structure can be widely in VLSI design area, like computer aided design for VLSI (electronic design automation), chip design, and wafer foundry, to raise yield.
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