國立臺灣大學技術行銷表

台大案號:_06A-100716_（由產學合作中心填寫）

產學合作中心聯絡人：蘇祈烈　電話：02-33669949　e-mail：such@yahoo.com.tw

產品/技術名稱	製造結晶型孔洞低介電係數層之方法
發明人/單位	萬本儒，呂信諺，鄧志霖，龔建豪，游竣偉，柳佑樵及余俊賢/台灣大學化工系
產品/技術說明	本發明是為了製備薄膜表面型態平整且介電值小於 2 的 MFI 結晶型沸石低介電常數薄膜。可解決半導體元件因尺寸縮小而產生的電阻-電容時間延遲之問題，且該材料機械強度高，可承受化學機械研磨程序。此本發明製程時間短，可大幅降低製備成本。
應用範圍	針對半導體 IC 製程
產品/技術優勢	1. 本發明製備中孔洞 MFI 結晶型沸石低介電常數薄膜，其機械強度高(彈性係數大於 10GPa，硬度大於 1GPa)，且介電常數低於 2。 2. 本發明改善過去利用 MFI 結晶型沸石顆粒之溶液當成鍍膜溶液所產生的表面形態極度不平整問題。 3. 本發明製備 MFI 結晶型沸石顆粒，且將顆粒的結晶度於一恰當的範圍，於此範圍內的顆粒所製備之中孔洞 MFI 結晶型沸石低介電常數薄膜擁有高機械強度。 4. 此本發明製程時間短，可大幅降低製備成本。 5. 本發明所使用的界面活性劑可使薄膜形成更多的孔洞，而降低介電常數。
市場潛力	ITRS2008(http://www.itrs.net/)年所公佈的半導體需求顯示，當半導體製程邁向 32 奈米時，低介電係數材料的介電係數必須在 2.4 以下，而到 20 奈米時(2015 年)，介電常數更需低至 1.9。而傳統所使用之介電材料離此目標仍有大段距離，因此可以肯定此材料於未來具有高度的應用潛力。
產品/技術 智財權保護方式	專利申請中

Marketing Abstract of NTU's Invention Disclosure

NTU's docket no: 06A-100716 (由產學合作中心填寫)

CIAC contact：蘇祈烈 Tel：02-33669949 e-mail：such@yahoo.com.tw

Title	Methods for manufacturing crystalline porous low-k films
Inventor (s)	Ben-Zu Wan, Hsin-Yan Lu, Chin-Lin Teng, Chien-Hao Kung, Chun-Wei Yu, Yu-Chiao Liu, and Chun-Hsien Yu/ Department of Chemical Engineering, National Taiwan University
Brief Description	This invention includes methods for preparing MFI-type zeolite low dielectric (low *k* value) films with flat surface morphology, *k* values of < 2, and high mechanical strength. A *k* value of < 2 is able to address the problem of resistive-capacitive (RC) time delay as the size of the elements in IC chips continuous to shrink. Furthermore, the films prepared in this invention possessed high mechanical strength which is strong enough to withstand high torque during the process of chemical mechanical polishing (CMP). The whole process to prepare the films is short, reducing production costs.
Fields of Application	The industry of integrated circuit (IC) manufacturing
Advantages	1. Disclosed in this invention, mesoporous MFI-type zeolite low dielectric (low *k* value) films with smooth surface morphology, *k* values of < 2, and high mechanical strength (an elastic modulus of > 10GPa, and a hardness of > 1GPa) have been prepared successfully. 2. MFI-type zeolite low *k* films with flat surface morphology were obtained with the methods disclosed in this invention. 3. By turning the crystallinity of MFI-type zeolite nanoparticles, one can prepare the films with high mechanical strength from the resulting nanoparticles. 4. The whole process to prepare the films is short, reducing production costs. 5. Surfactants used in this invention were for forming more pores inside the films after those were removed, reducing the *k* values of the films.
Market Potential	ITRS 2008 established that the required value of the dielectric constant (*k* value) will be 1.9 as the gate length of CMOS devices approaches 20 nm in 2015. However, the *k* value of the traditionally used intermetal dielectric, dense silica, is around 3.9, which is still far away to meet the required value. Therefore, it is definitely sure that the low-k film synthesized in this study is highly competitive.
IP Right(s)	Patent pending