連接電子元件之結構

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市場及需求:

- 半導體製造公司(TSMC, Intel, SAMSUNG, Qualcomm)
- 半導體封裝測試公司(ASE, SPIL)

技術摘要(含成果):

近年來，電鍍銅柱凸塊的技術已經逐漸成熟。相對於目前廣泛使用的無鉛銲錫凸塊，電柱銅柱凸塊更適合用於微小線距的條件，以達到更高的封裝密度及更高功能的晶片；但目前電鍍銅柱凸塊的接合還是必須仰賴少許的銲錫，隨著銅柱的直徑不斷縮小，小體積的銲錫會在接合完畢或是使用一段時間後轉變為全介金屬的銲點，當結構中不再具有柔軟的銲錫吸收應力，晶片容易在 low-k 曾發生破壞。因此本發明結合無電鍍的技術並透過外加流場的方式提供銅柱全金屬的接合，以確保晶片的銲點在接合完畢後不會生成堅硬的介金屬。

優勢:

(1) 低溫製程(< 90℃)。
(2) 製造過程不需加壓。
(3) 避免易脆之 IMC joint 及 micro void 產生。
(4) 能夠彌補錯位造成的影響。

競爭產品:

(1)錫球銲點。
(2)US2008/0073795A1。

專利現況:

本技術已有相關專利（中華民國專利申請號: 105105177；美國專利申請號: 14/802,903）。

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Interconnection structures for making the same

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Market Needs:

- Semiconductor manufacturing companies (TSMC, Intel, SAMSUNG, Qualcomm)
- Semiconductor packaging and testing companies (ASE, SPIL)

Our Technology:

Cu pillar bump offers more advantages comparing with conventional solder bump and is gradually becoming the next generation bumping technology for fine pitch applications. However, while the diameter of Cu pillar decrease, smaller Cu pillar solder-cap volume poses adverse effects on reliability. The most critical issue is that full-IMC joints could degrade the mechanical stability of the Cu/low k structure due to the increase in the driving force for fracture.

In this study, to overcome this problem and optimize performance, we developed a new bonding technology that utilizes electroless metal deposition with the application of external pressure on the plating solution to replace solders and directly bond pillars.

Strength:

(1) Low-temperature process(< 90°C)。
(2) Pressureless process.
(3) Avoid the formation of brittle IMS and micro voids.
(4) Compensate for misalignment.

Competing Products:

(1) Tin-based solder joints.
(2) US2008/0073795A1.

Intellectual Properties:

This technique is protected by ROC patent 105105177 and US patent 14/802,903.

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