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(54) **PHASE LOCKED LOOP CAPABLE OF FAST LOCKING**  
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(\* ) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 898 days.

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See application file for complete search history.

(57) **ABSTRACT**  
A phase locked loop includes a voltage controlled oscillator operable to generate an output signal corresponding to a reference signal in response to a control voltage signal outputted by a filter in response to a current signal, and a variable frequency divider operable to perform frequency division on the output signal using a variable divisor so as to generate a divided feedback signal. A charge pump outputs the current signal in response to a phase detecting output from a phase/frequency detector indicating phases of the divided feedback signal and the reference signal. A phase error comparator outputs, in accordance with the phase detecting output, a digital output indicating whether the divided feedback signal lags or leads the reference signal and further indicating a phase difference between the divided feedback signal and the reference signal. The variable frequency divider determines a value of the variable divisor in accordance with the digital output to reduce the phase difference between the divided feedback signal and the reference signal.

14 Claims, 10 Drawing Sheets

