US011112845B2

(12) **United States Patent**
Shih et al.

(10) **Patent No.: US 11,112,845 B2**
(45) **Date of Patent: Sep. 7, 2021**

(54) **PROBABILISTIC FRAMEWORK FOR COMPILER OPTIMIZATION WITH MULTITHREAD POWER-GATING CONTROLS**

(71) Applicants: **National Taiwan University**, Taipei (TW); **MEDIATEK INC.**, Hsin-Chu (TW)

(72) Inventors: **Wen-Li Shih**, Taipei (TW); **Jenq-Kuen Lee**, Hsinchu (TW); **Cheng-Yen Lin**, Chiayi County (TW); **Ming-Yu Hung**, Nantou County (TW)

(73) Assignees: **National Taiwan University**, Taipei (TW); **MEDIATEK INC.**, Hsin-Chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/964,592**

(22) Filed: **Dec. 10, 2015**

(65) **Prior Publication Data**

US 2016/0378444 A1 Dec. 29, 2016

Related U.S. Application Data

(60) Provisional application No. 62/183,757, filed on Jun. 24, 2015.

(51) **Int. Cl.**
G06F 1/28 (2006.01)
G06F 8/41 (2018.01)

(52) **U.S. Cl.**
CPC ***G06F 1/28*** (2013.01); ***G06F 8/4432*** (2013.01); *Y02D 10/00* (2018.01)

(58) **Field of Classification Search**
CPC G06F 1/32–3296; G06F 8/00–78; G06F 1/329–3296; G06F 8/4432; G06F 1/3234–3296; G06F 1/28; Y02D 10/00
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

2003/0014742 A1* 1/2003 Seth G06F 8/443 717/158
2006/0277509 A1* 12/2006 Tung G06F 17/5022 716/109

(Continued)

OTHER PUBLICATIONS

Corbet, "Counting on the time stamp counter", Posted Nov. 13, 2006. https://lwn.net/Articles/209101/. Retrieved Jul. 8, 2019 (Year: 2006).*

(Continued)

Primary Examiner — Doon Y Chow
Assistant Examiner — Joanne G Macasiano
(74) *Attorney, Agent, or Firm* — Winston Hsu

(57) **ABSTRACT**

A probabilistic framework for compiler optimization with multithread power-gating controls includes scheduling all thread fragments of a multithread computer code with the estimated execution time, logging all time stamps of events, and sorting and unifying the logged time stamps. Time slices are constructed using adjacent time stamps of each thread fragment. A power-gating time having a component turned off for each time slice is determined. Power-gateable windows that reduce energy consumption of the time slice is determined according to the power-gating time. The compiler inserts predicated power-gating instructions at locations corresponding to the selected power-gateable windows into the power-gateable computer code.

9 Claims, 11 Drawing Sheets