US008671375B1

(12) **United States Patent**
Chung et al.

(10) **Patent No.: US 8,671,375 B1**
(45) **Date of Patent: Mar. 11, 2014**

(54) **FUNCTIONAL TIMING ANALYSIS METHOD FOR CIRCUIT TIMING VERIFICATION**

(71) Applicant: **National Taiwan University**, Taipei (TW)

(72) Inventors: **Yi-Ting Chung**, Taitung County (TW); **Jie-Hong Jiang**, Taipei (TW)

(73) Assignee: **National Taiwan University**, Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **13/672,760**

(22) Filed: **Nov. 9, 2012**

(51) **Int. Cl.**
G06F 9/455 (2006.01)
G06F 17/50 (2006.01)

(52) **U.S. Cl.**
USPC **716/113**; 716/106; 716/134

(58) **Field of Classification Search**
USPC 716/106, 108, 113, 134
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,086,626 A * 7/2000 Jain et al. 716/103
6,615,395 B1 * 9/2003 Hathaway et al. 716/113
6,714,902 B1 * 3/2004 Chao et al. 703/14
7,363,605 B1 * 4/2008 Kondratyev et al. 716/113
7,742,907 B2 * 6/2010 Gupta et al. 703/14
2005/0097484 A1 * 5/2005 Sarwary et al. 716/6
2007/0299648 A1 * 12/2007 Levitt et al. 703/22
2008/0201671 A1 * 8/2008 Rejouan et al. 716/6
2008/0288904 A1 * 11/2008 Rahim et al. 716/6
2009/0132984 A1 * 5/2009 Chander et al. 716/6

* cited by examiner

Primary Examiner — Thuan Do
Assistant Examiner — Brian Ngo
(74) *Attorney, Agent, or Firm* — Li & Cai Intellectual Property (USA) Office

(57) **ABSTRACT**

A functional timing analysis method, executed in a computing device, comprises: step A: obtaining a circuit; step B: selecting a target delay time from a delay time set for a node in the circuit for verifying whether the target delay time is attainable by some input assignment; step C: generating a timed characteristic function associated with the selected target delay time for the node recursively from the timed characteristic functions associated with the corresponding delay times for its fanin nodes is generated as a target formula; step D: recursively translating the timed characteristic function into timed characteristic function clauses of the target formula by using an implication operator; step E: checking whether the target formula is satisfied by using a Boolean satisfiability solver; and step F: if the target formula is satisfied, the selected target delay time is attainable by some input assignment to the circuit.

10 Claims, 3 Drawing Sheets